REMARKS

In response to the Office Action mailed on February 22, 2006, Applicant wishes to enter the following remarks for the Examiner's consideration. Claims 1-36 are pending in the application; claims 2, 18 and 32 have been canceled without prejudice.

Rejection of claims

Claims 1, 9, 31, 34-35 are rejected under 35 USC §102(e) as being anticipated by Ao (US 6,987,683). Claims 14-15 are rejected under 35 USC 103(a) as being unpatentable over Ao in view of Schultz et al. (US 5,995,401). Claims 17, 19, 36 are rejected under 35 USC 102(a) as being anticipated by Ao or in the alternative over Lin (US 5,422,838).

Applicant as amended base claims 1, 17, and 31 to include the recitation of allowable claims 2, 18 and 32, respectively. As such it is believed that claims 1-16, 17-20 and 31-33 now define allowable claims.

A distinction seen between the claimed invention and the Ao reference is the present invention uses a bit slice approach in which each CAM bit cell has its own circuit for the bit slice comparator. This comparator portion of the bit cell works more like an adder circuit in that a carry signal is fed from least significant bit cells to higher significant bit cells. This integration of CAM bit cell and comparator bit cell makes for a highly refined cell layout, reducing area and improving performance.

The present invention thus makes use of carry (or "previous magnitude signal") signals. The carry signals allow both less than and greater than operations to be performed simultaneously. For This provides, for a very small price in area, complete magnitude CAM functionality which Ao's approach does not do. This is an advantage.

The Ao reference, conversely, takes a wholly different approach. Ao requires one operation be done at a time through the comparator, then the configuration is changed for a different operation. The reason for this different is the architecture. Ao uses a stand alone comparator using combination logic comprised of several stages of logic gates that have many inputs and one or more outputs. Each data bit from the CAM bit cell and compare bit from its register feed the comparator. For example, Ao shows a five bit comparator. If the compare word is larger than five bits then more than one fib-bit comparator can be cascaded to another comparator. This cascading can continue until all bits in the word are compared and a single result produced. Physically, these comparators are not part of the CAM bit cell because the comparator logic gates do not repeat on a bit basis. This circuit will likely be placed next to the bit cells but will not be part o the CAM bit cell.

With regard to claims 34-36, Applicant respectfully traverses this rejection of the claims and respectfully submits the following. In keeping with the above description of the distinctions between the claimed invention and the Ao reference, it is to be noted that these claims do, in fact, reference the carry

nature of the comparator, discussed above. The comparator is integrated into the CAM bit cell as a comparator bit cell. When comparing each bit pair of two binary numbers, it is necessary to include information about the comparison of lower significant bit pairs. This information is carried on from bit pair to bit pair.

Ao's comparator, conversely, uses a separated circuit to do the comparison. The overhead for this approach is less efficient than that of the claimed invention.

This carry signal(s) distinction is found in claims 34-36. Claim 34, for instance, discusses "previously magnitude signal is generated by a second cell of the plurality of MCAM cells ..." Claim 36, directed to MCAM cells, recites that "the output magnitude signal of an MCAN cell magnitude comparator in the series arrangement is provided as the input magnitude signal to a subsequent MCAM cell magnitude comparator in the series arrangement...."

In light of the foregoing amendments and explanations, Applicant submits that all rejections of the claims have been overcome. Allowance of claims 1, 3-17, 19-30, 31 and 33-35 is therefore respectfully requested at the Examiner's earliest convenience. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion. The undersigned wishes to

make it clear that not making such arguments at this time should not be construed as a concession or admission to any statement in the Office Action.

Please contact the undersigned if you have any questions regarding this application.

Respectfully submitted,

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